

Fig.1

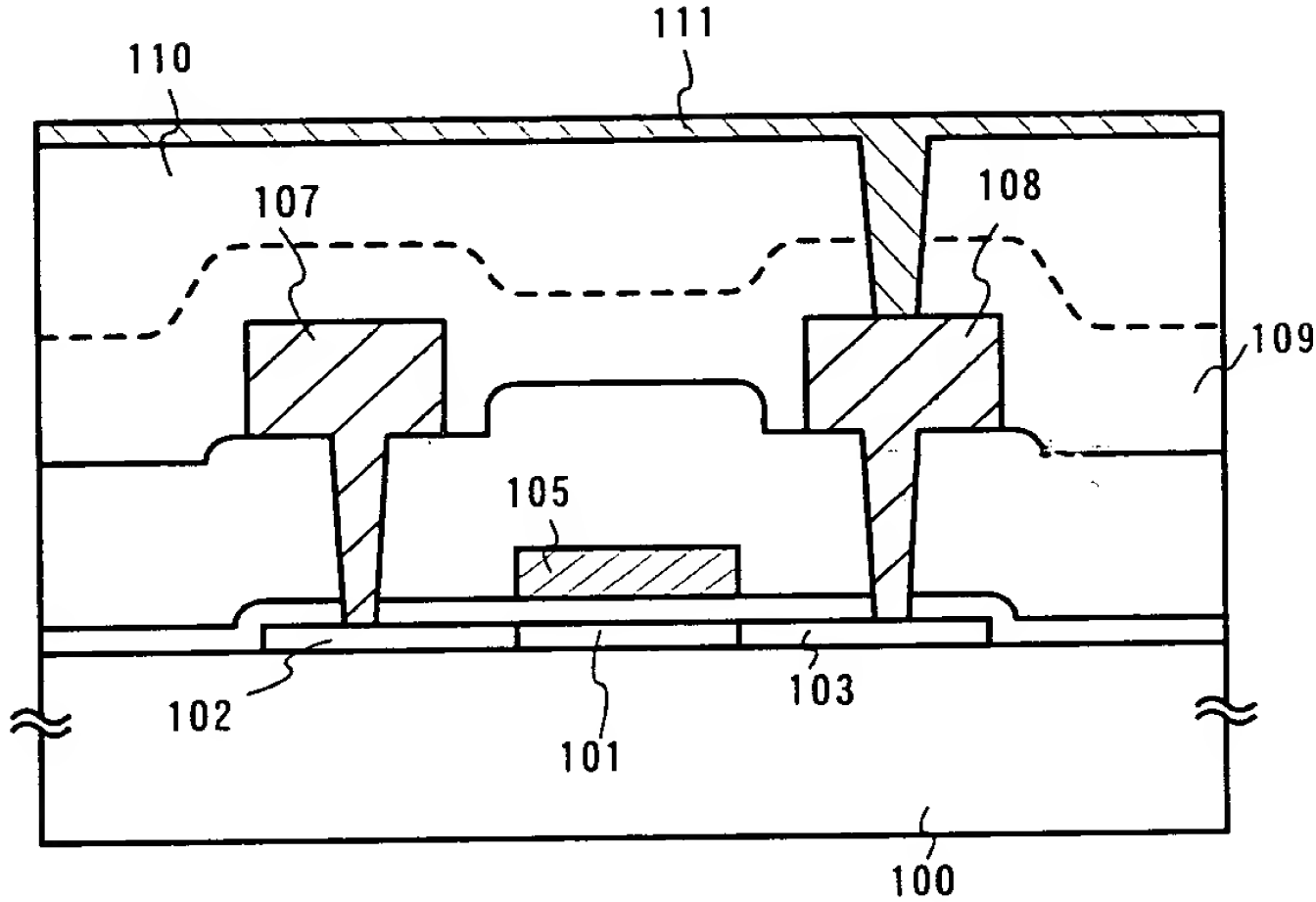


Fig.2

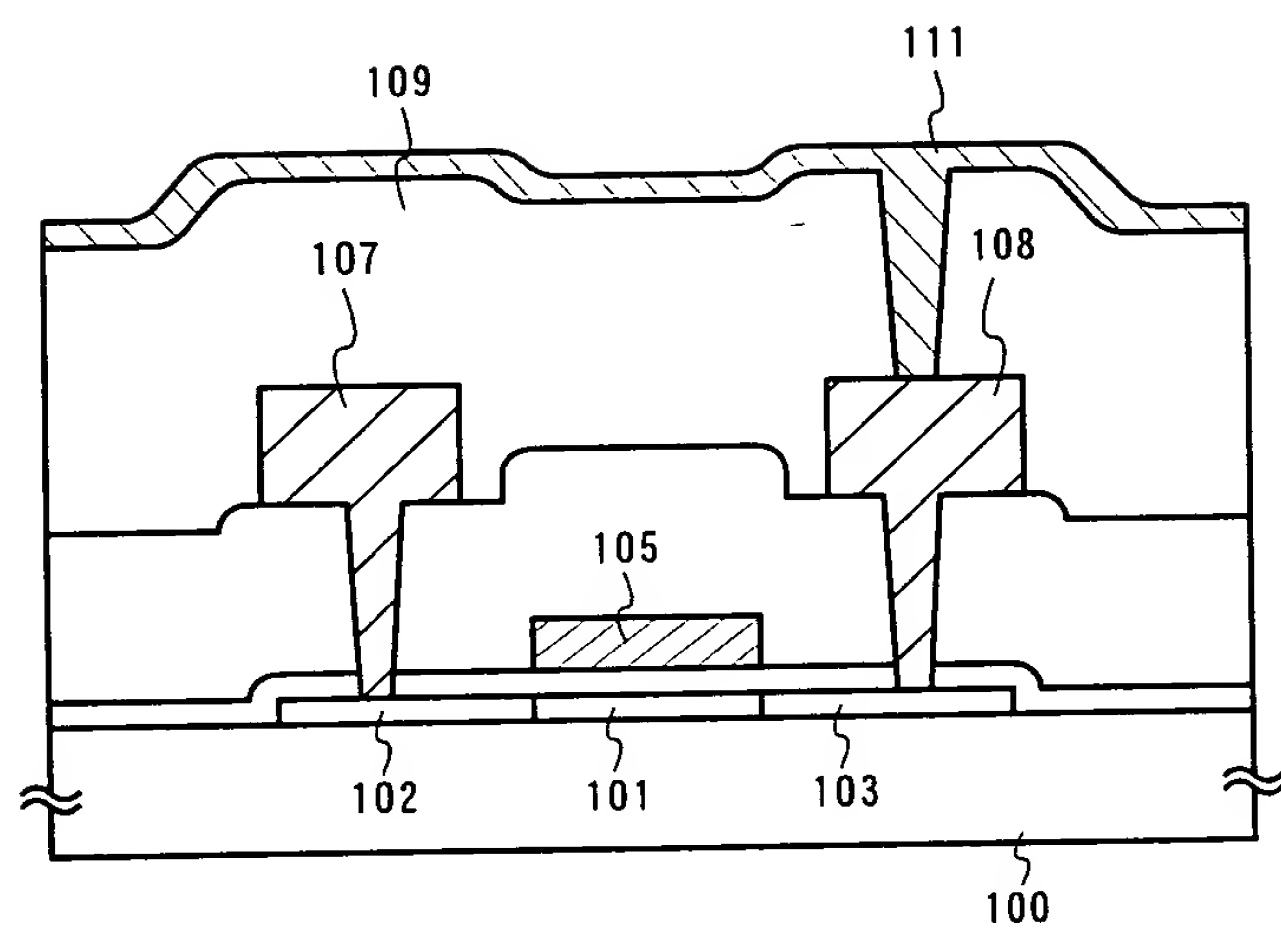


Fig. 2 is a cross-sectional view of a semiconductor device in accordance with the present invention. The device includes a substrate 100, a gate oxide layer 101, a gate electrode 102, a source/drain region 103, a channel region 105, a source/drain contact 107, a gate contact 108, and a source/drain contact 109. The device is shown in a cross-sectional view, with the substrate 100 at the bottom and the gate oxide layer 101 on top. The gate electrode 102 is formed on the gate oxide layer 101, and the source/drain region 103 is formed in the substrate 100. The channel region 105 is formed in the substrate 100, and the source/drain contact 107 is formed on the source/drain region 103. The gate contact 108 is formed on the gate electrode 102, and the source/drain contact 109 is formed on the source/drain region 103. The device is shown in a cross-sectional view, with the substrate 100 at the bottom and the gate oxide layer 101 on top.

Fig.3

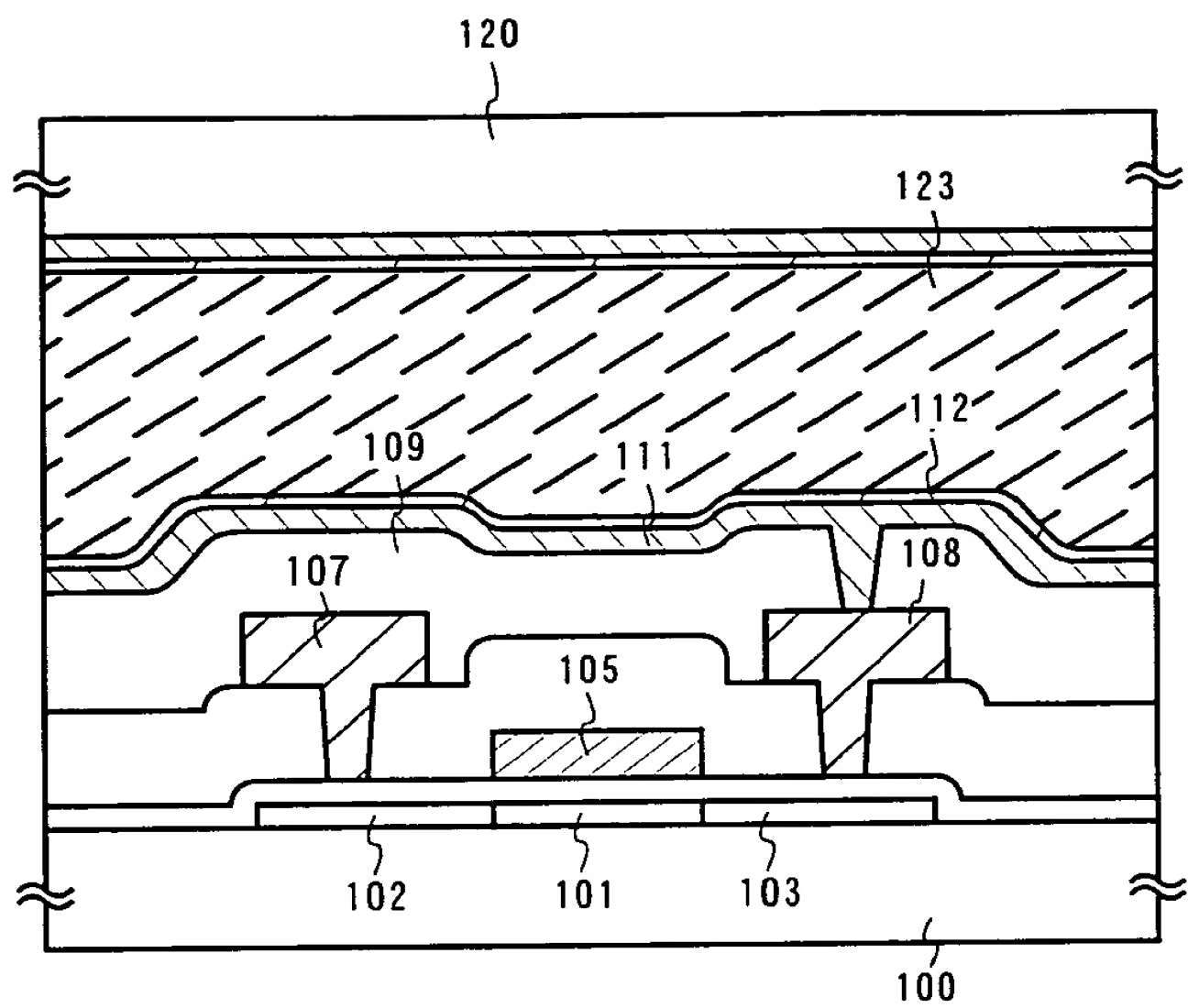


Fig.4

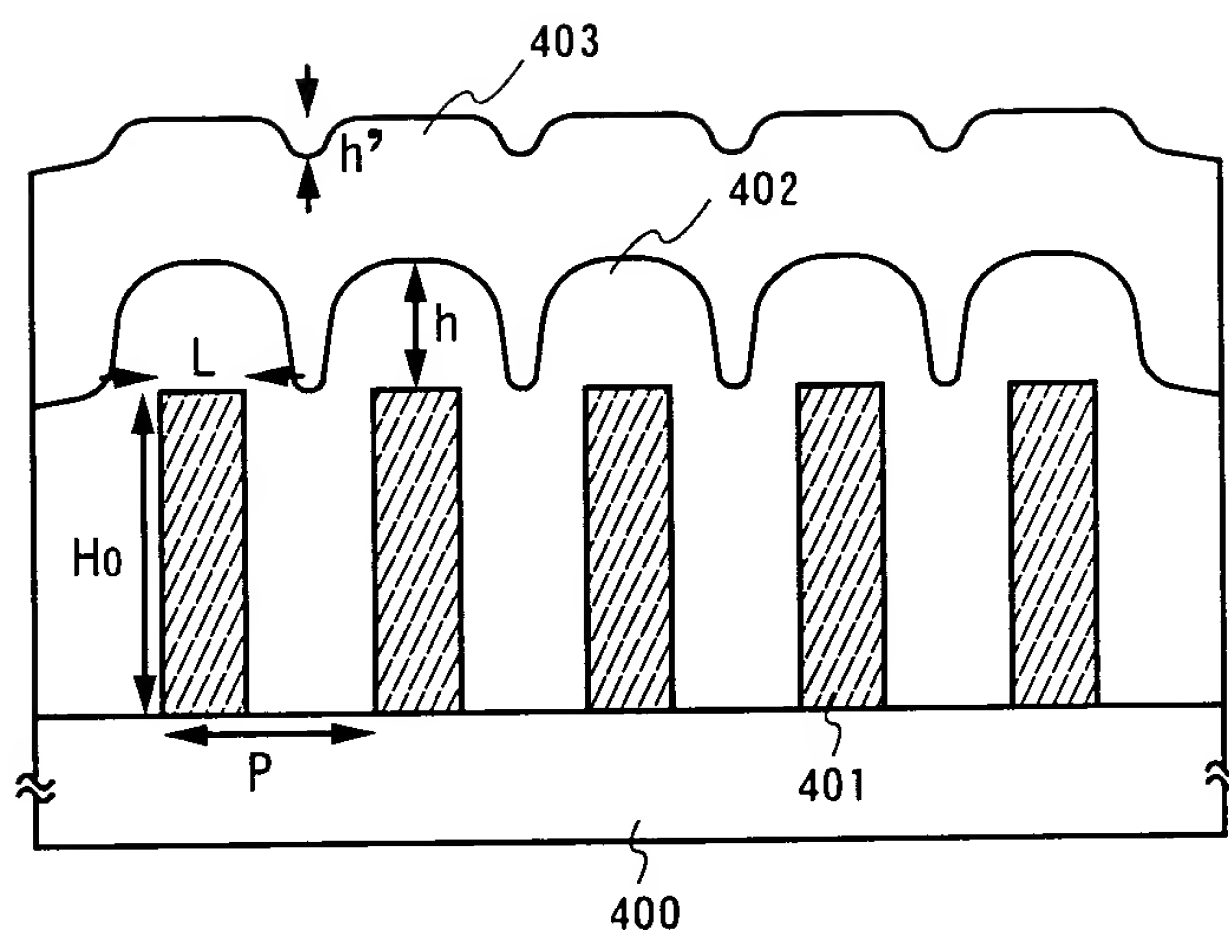


Fig. 5

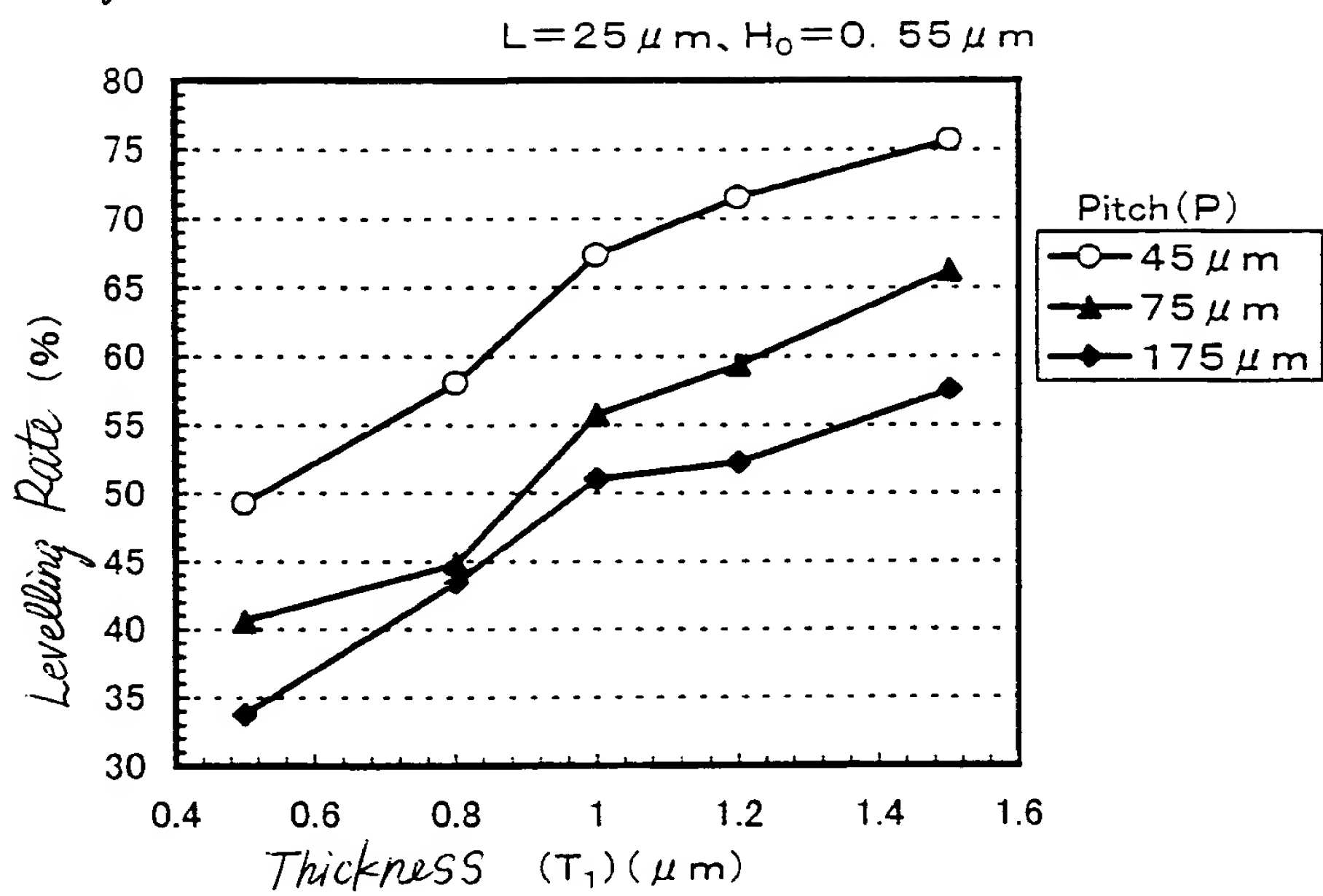
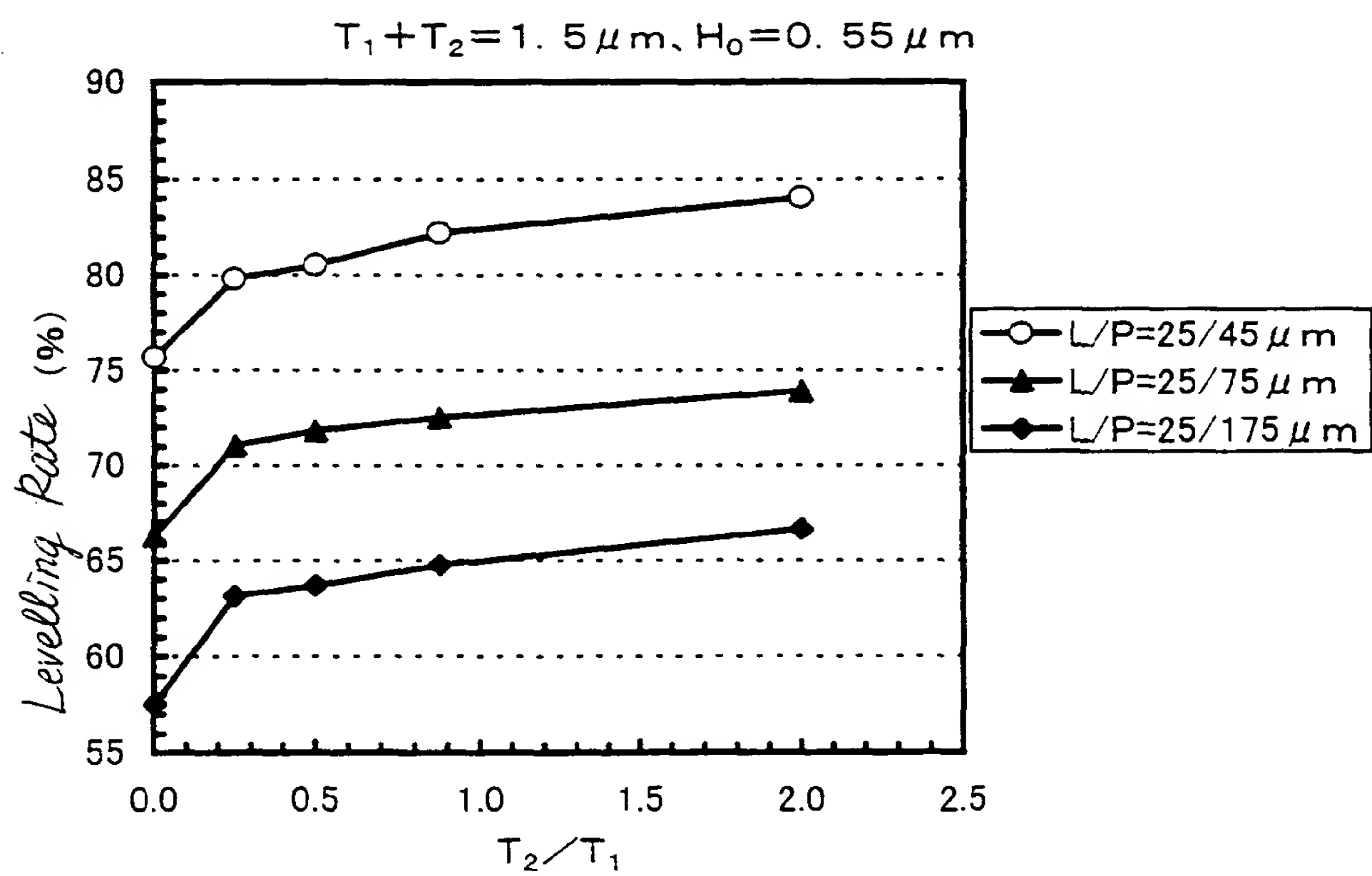
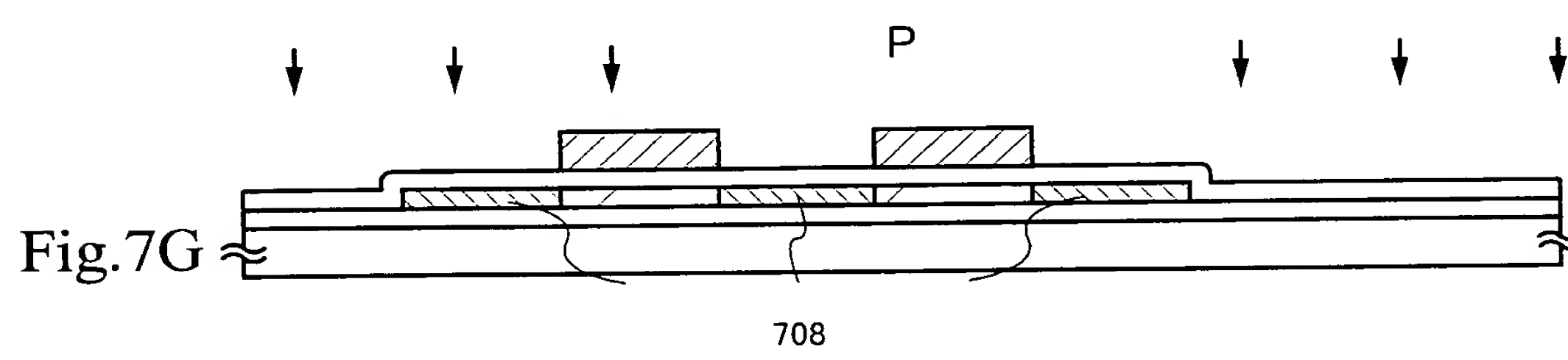
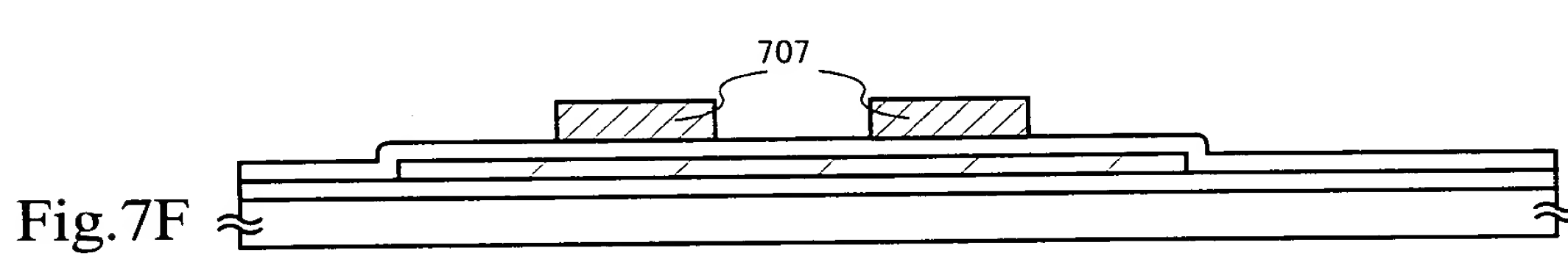
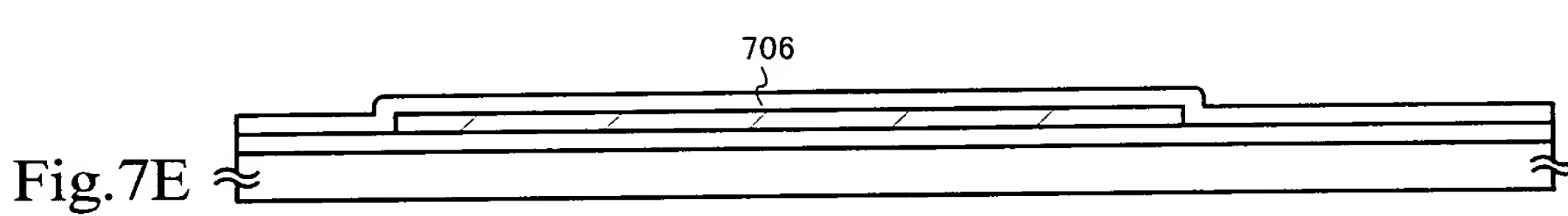
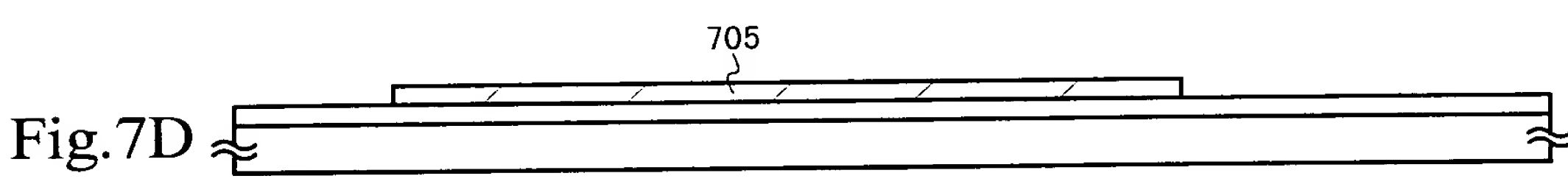
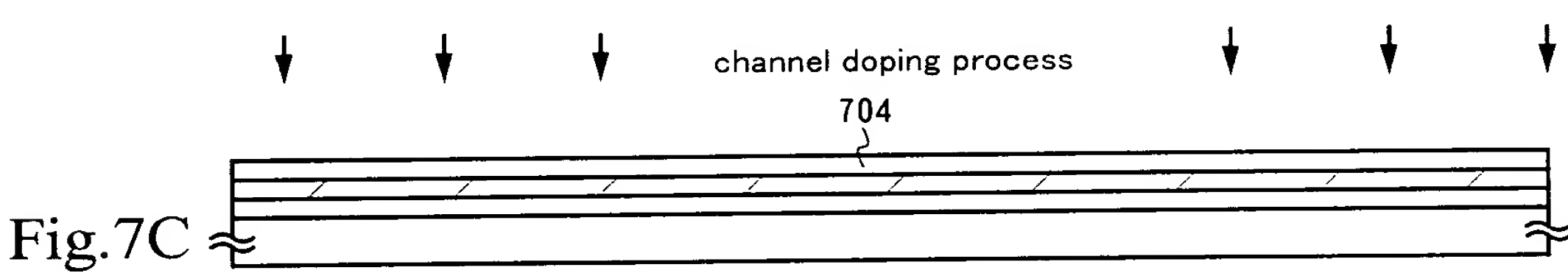
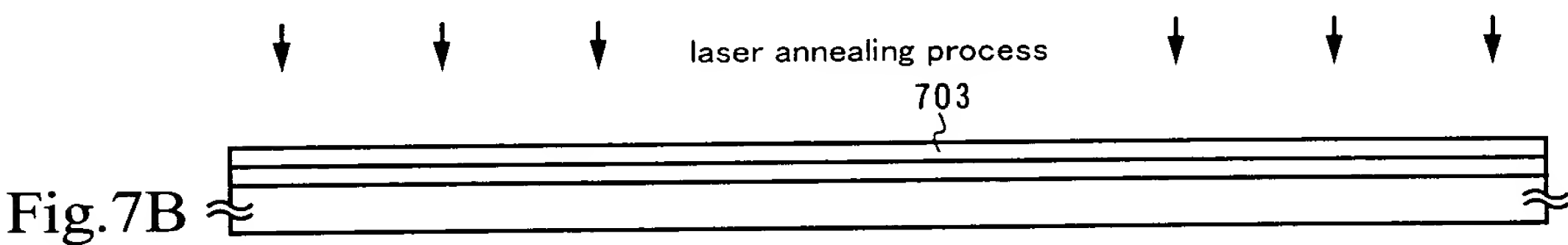
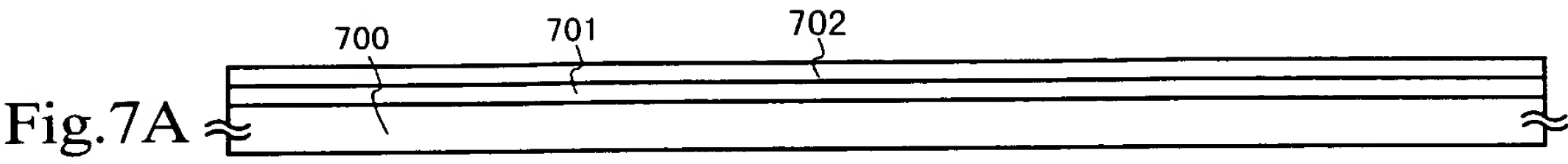
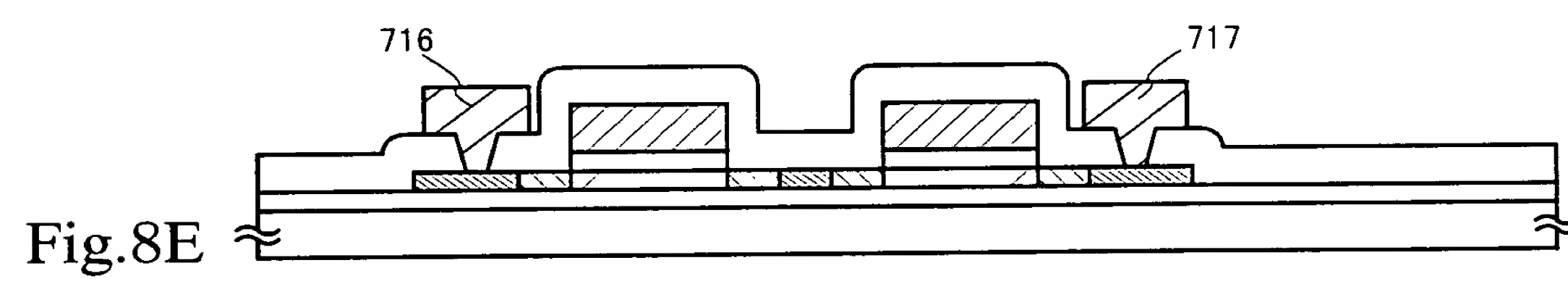
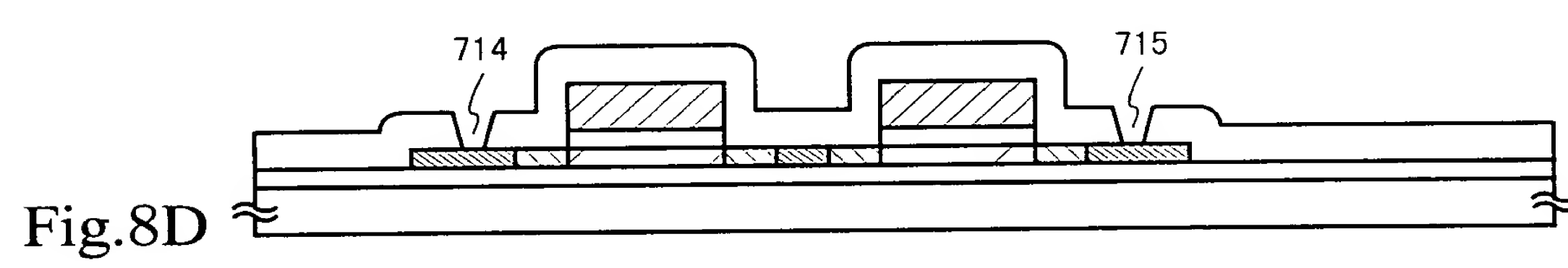
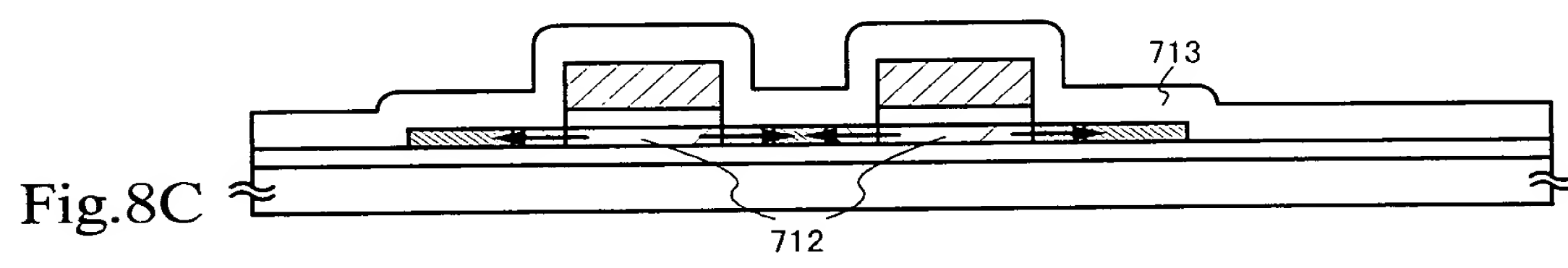
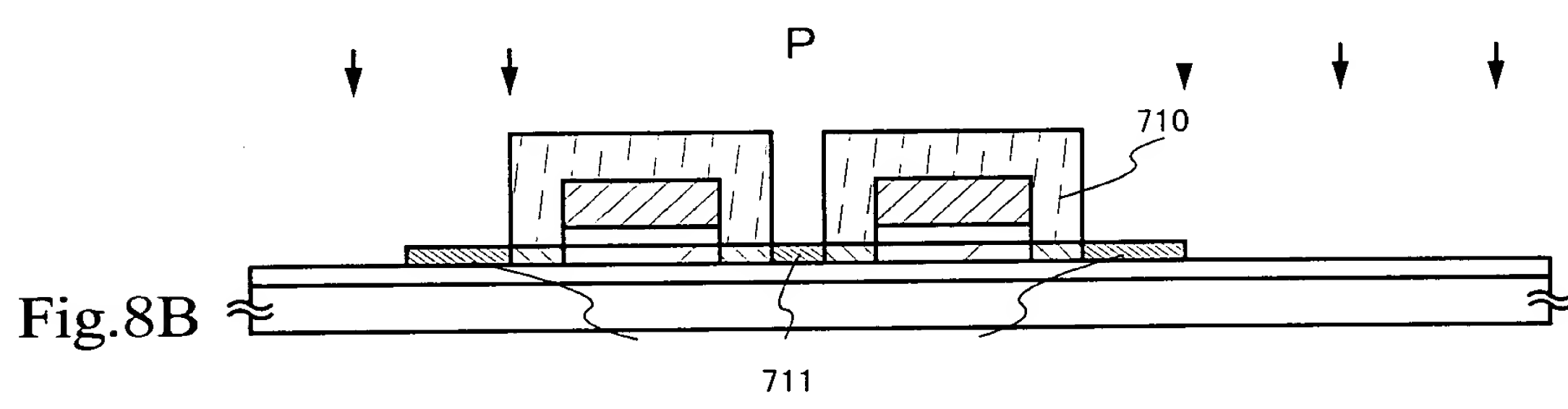
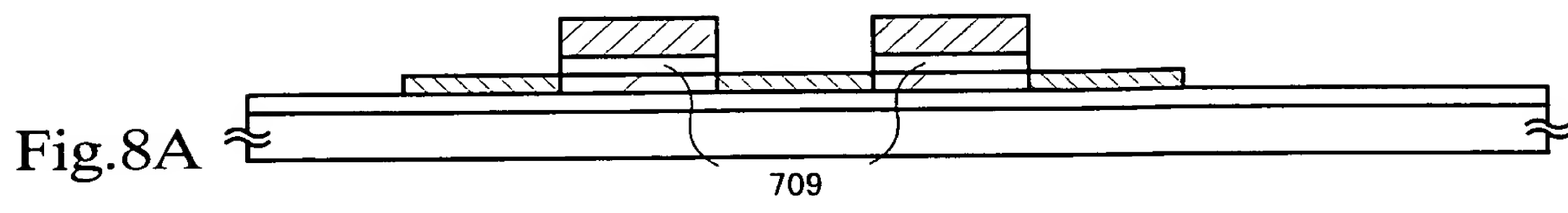


Fig. 6









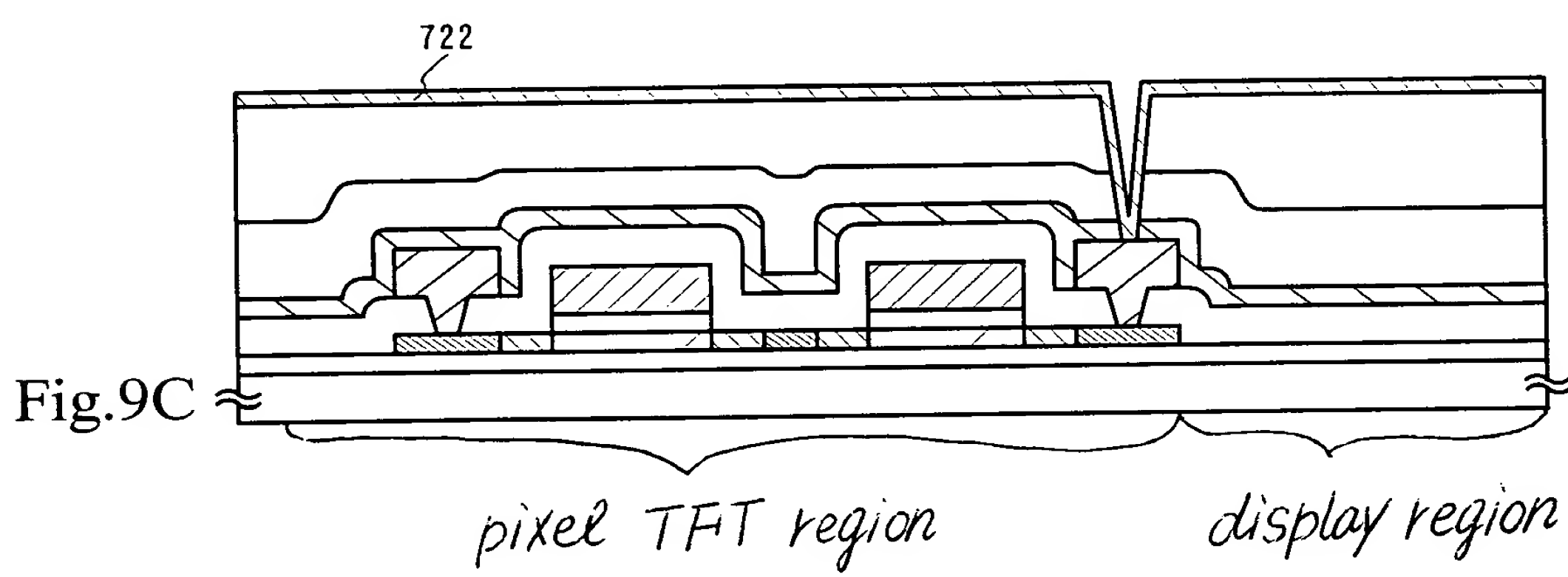
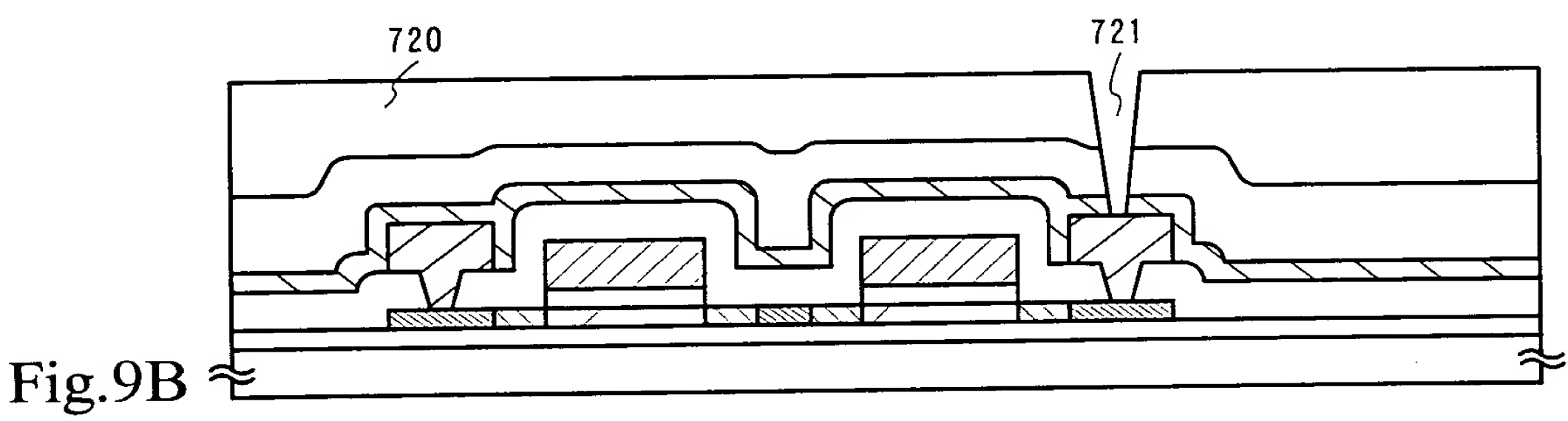
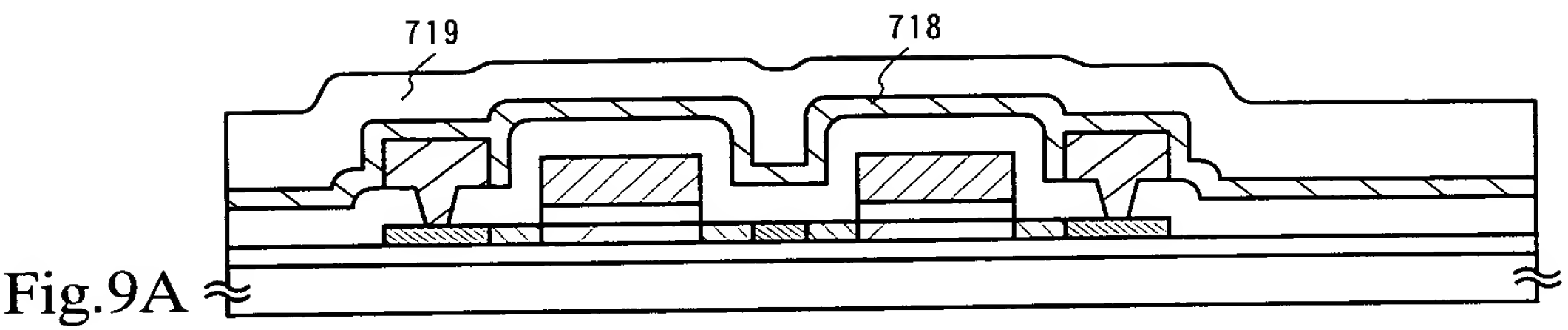


Fig.10

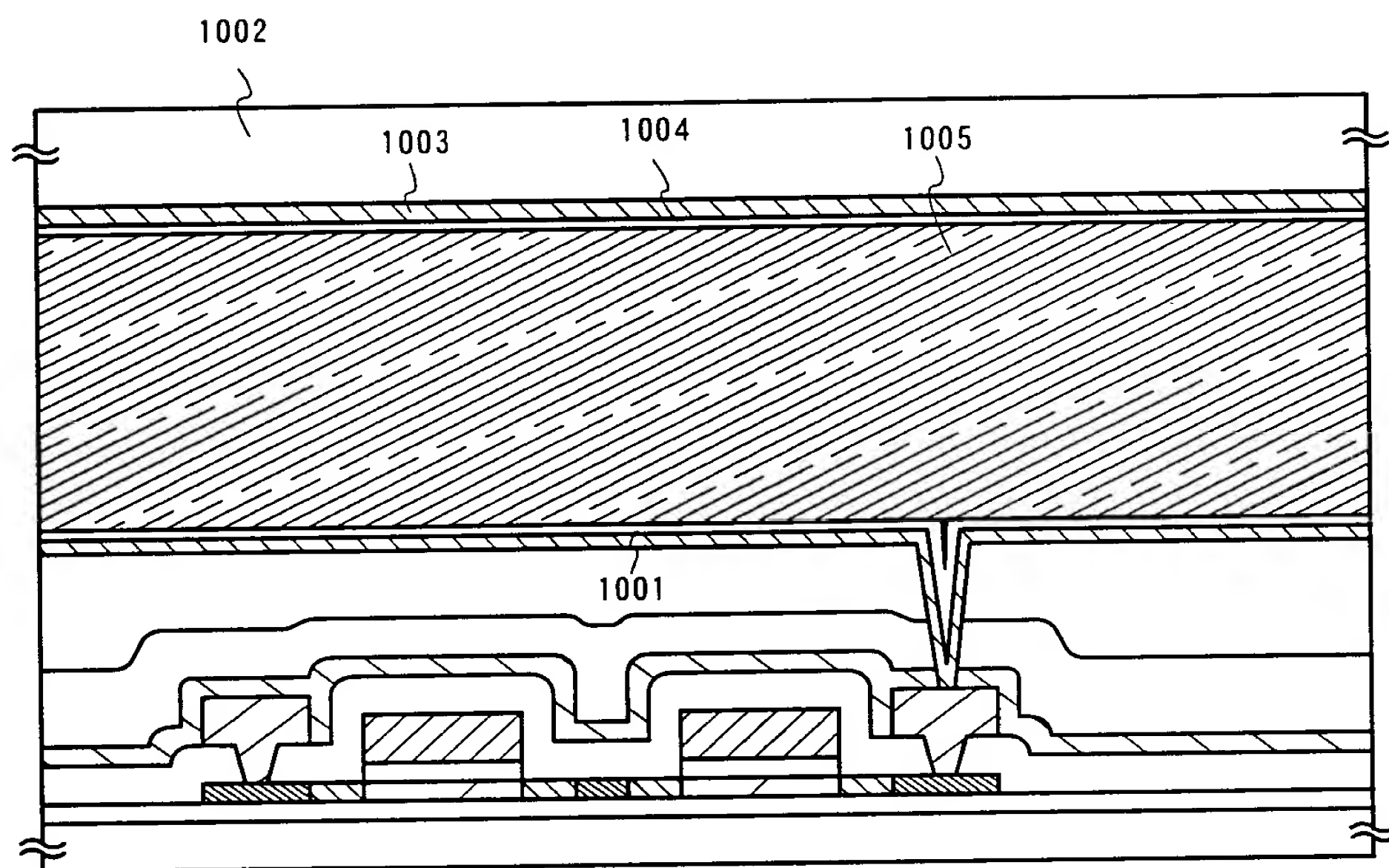


Fig. 11

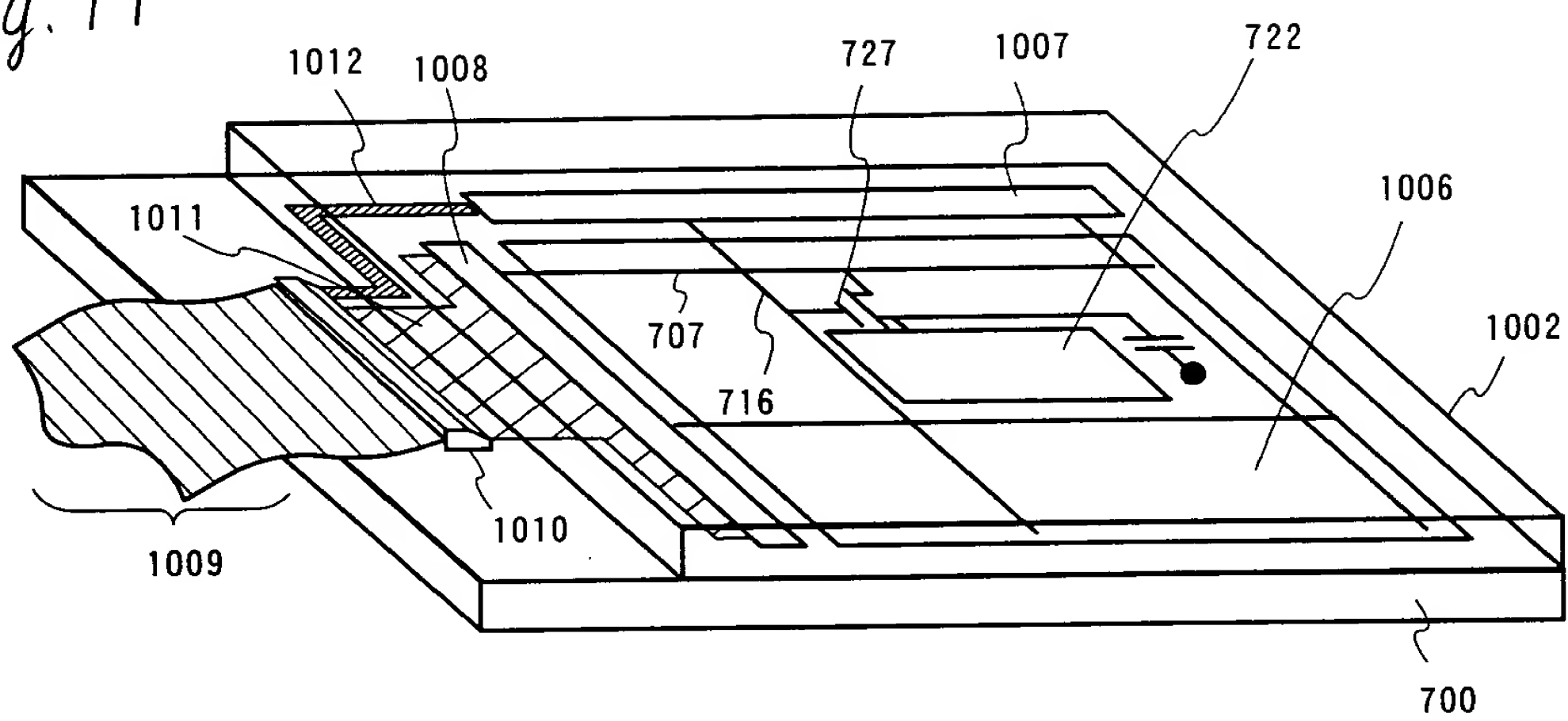
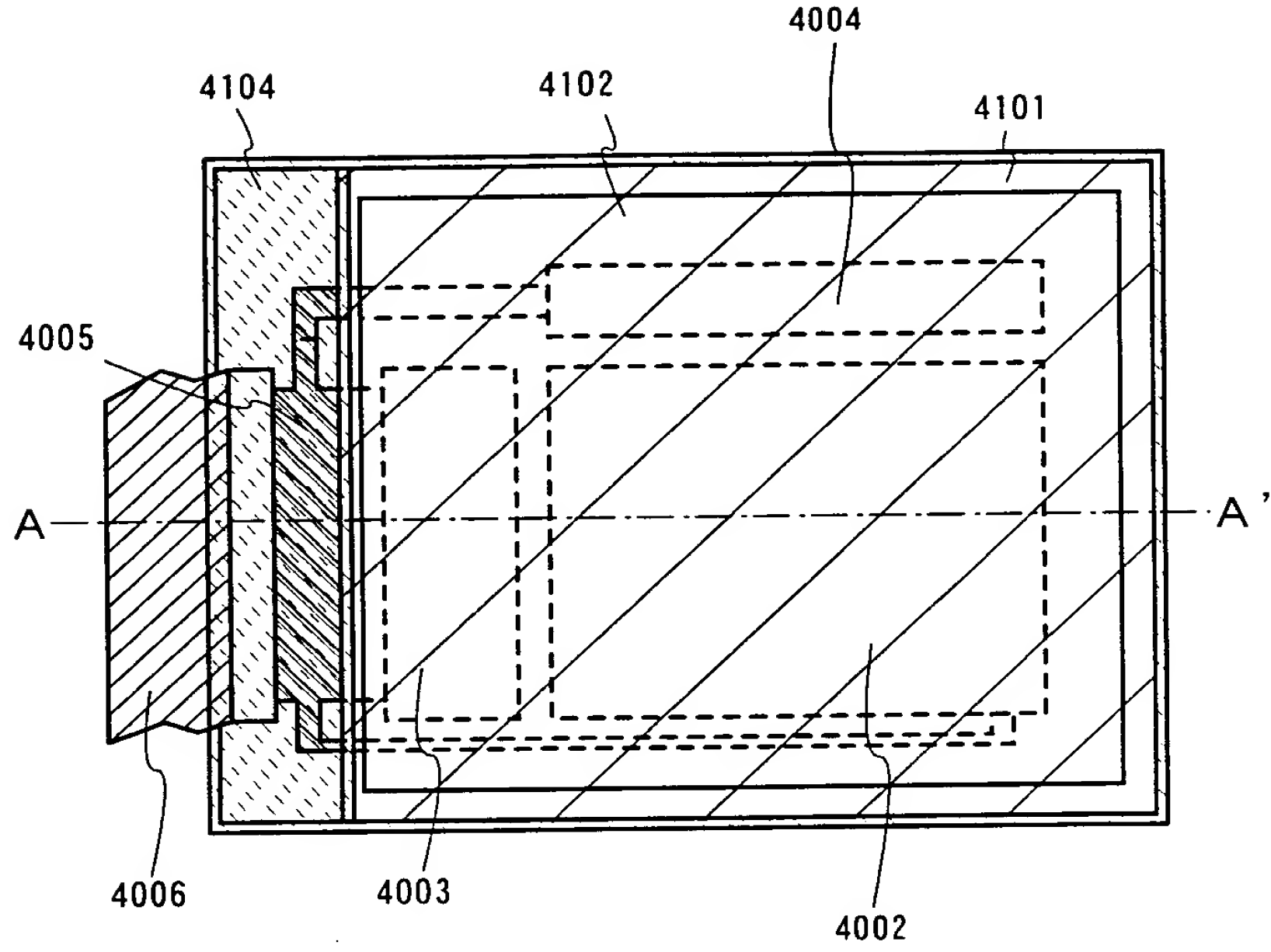


Fig.12



Fig,13

